



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Cc
APPLICATION NO.

FILING DATE

FIRST NAMED INVENTOR

ATTORNEY DOCKET NO. *JK*

09/090,096 06/03/98 CHUI

G 81862.P096

TM11/1024

BLAKELY SOKOLOFF TAYLOR AND ZAFMAN
12400 WILSHIRE BOULEVARD
7TH FLOOR
LOS ANGELES CA 90025

EXAMINER

LOGSDON, J

ART UNIT

PAPER NUMBER

2662 *b*

DATE MAILED: 10/24/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)
	09/090,096	CHUI ET AL.
	Examiner Joe Logsdon	Art Unit 2662

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) _____ is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-49 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
 - a) All b) Some * c) None of the CERTIFIED copies of the priority documents have been:
 1. received.
 2. received in Application No. (Series Code / Serial Number) _____.
 3. received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

- | | |
|---|--|
| 15) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 18) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 16) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 19) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 17) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 20) <input type="checkbox"/> Other: _____ |

Claim Rejections—35 U.S.C. 112, First Paragraph:

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-49 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1, 34, and 42 include the limitation that a cell size of each of the unidirectional buffers is programmable. According to common usage a cell is a fixed length unit of transmission used by ATM. The word “cell” is therefore used to describe a unit of transmission rather than a property of a buffer. Applicant fails to define “cell” as it pertains to a description of the buffers. The disclosure therefore does not enable one of ordinary skill in the art to either make or use the invention.

Applicant can use applicant's own terminology—provided that any unusual words are defined in the specification. On page 30, line 27 to page 31, line 3, it is stated, “Programmable parameters are used to customize the FIFO 2900, wherein the cell size, or number of words per cell,...” This statement defines “cell size” as it pertains to the buffer as being the “number of words per cell.” One of ordinary skill in the art knows what “word” means. But the latter “cell” is still left undefined. For example, one may interpret the latter “cell”, according to common usage, to mean the unit of transmission used for ATM; the ATM cell size is fixed, so if the word size is programmable (as it is according to at least one embodiment of the invention) then the “cell size” must also be programmable.

The intended meaning of the term “cell” as it applies to the buffers is particularly unclear in light of the description on page 31. In lines 10-11 it is stated, “A cell size of the first and second unidirectional FIFO buffers is programmable.” Two sentences later, in the same paragraph, it is stated, “The bidirectional FIFO unit is coupled to write at least one cell from and read at least one cell to at least one asynchronous transfer mode (ATM) interface,...” In the next sentence it is stated, “As such, the first unidirectional FIFO buffer is coupled to write at least one cell from...a frame relay interface...” The word “cell” in the first sentence pertains to the buffers. In the second sentence, the word “cell” could pertain to either the buffers or the ATM stream, although it is more reasonable to interpret it in terms of the ATM stream. In the third sentence, the word “cell” seems more likely to pertain to the buffers because, according to common usage, frame relay does not employ cells; but because the specification describes all traffic as “cell traffic,” it appears that applicant may have defined the word “cell” so that it describes the unit of transmission used by frame relay. A third possible interpretation for the third sentence—and the one which is adopted below because it seems most reasonable—is that the frame relay interface is actually a frame relay to ATM interface that transforms frame relay packets to ATM cells and vice versa.

Evidence that applicant intends “cell” to have the same meaning in the context of the buffers as in the context of the communication traffic can be found, for example, on page 17, lines 20-21, where it states, “If the number of cells in the egress FIFO of the target reaches a threshold, the ECP discards the incoming cell.” Because applicant has failed to explicitly define “buffer cell size,” it is therefore assumed in what follows that applicant intends “cell” as used in the expression “buffer cell size” to have the same meaning as “cell” as used in “ATM cell.”

Claim Rejections-35 U.S.C. 112, Second Paragraph:

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 23 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 23 and 24, which depend on claim 22, recite the term “the write port cell count.” According to claim 22, each unidirectional FIFO buffer outputs a write port cell count. It is therefore unclear to which of the unidirectional FIFO buffers the term “the write port cell count” is intended to refer in claims 23 and 24.

5. Claims 34-41 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Claim 34 recites “A network switch platform comprising ... at least one discard enable signal.” It is obvious to one of ordinary skill in the art that a network platform cannot comprise a signal. Claims 35-41 depend on claim 34 and are thus similarly rejected.

Claim Rejections—35 U.S.C. 103(a):

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1-3, and 20-22, 25-32, 42-45, 47, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi et al. in view of Parry.

With regard to claims 1, 3, 42, and 43, Takamichi et al. discloses an apparatus comprising at least one bidirectional FIFO unit, wherein each such bidirectional FIFO unit comprises a first and second unidirectional FIFO buffer (Fig. 6; column 6, lines 28-32; cell buffer pairs 51-55, 7-8, and 61-65). As discussed above, the limitation that a cell size of each of the FIFO buffers is programmable is interpreted in what follows to mean that the word size of each of the FIFO buffers is programmable. Takamichi et al. fails to disclose an invention for which the buffer word size is programmable. Parry teaches a FIFO buffer that is useful for ATM applications and

whose word size can be programmed by either using more than one FIFO or varying the width of the input data bus (Fig. 3; column 13, lines 23-39). It would have been obvious to one of ordinary skill in the art to modify the invention of Takamichi et al. so that the word size of each of the FIFO buffers is programmable, as in Parry, because such a modification allows the invention to be used on a larger number of servers because servers vary in the word size they handle.

With regard to claims 2, 26, 28, 44, and 45, Takamichi et al. fails to address the issue of the timing of the read and write ports. Parry teaches that in a synchronous FIFO separate read and write clocks are used for the read and write ports, respectively (column 1, lines 54-57; column 5, lines 53-64; column 6, lines 44-55). Because they use separate clocks, the read and write ports are asynchronous with respect to each other. It would have been obvious to one of ordinary skill in the art to design the system of Takamichi et al. so that the read and write ports use read and write clocks, and that the read and write clocks are asynchronous with each other, as in Parry, so that activities within the switching platform can be coordinated and so that the switch can perform two non-interfering activities, such as reading from one buffer and writing to the other buffer, simultaneously and at different rates.

With regard to claims 22, 25, and 48, Takamichi et al. fails to disclose an invention for which each unidirectional buffer outputs a signal that indicates space available for at least one more cell in the unidirectional FIFO buffer or for which each unidirectional buffer outputs a signal that indicates that at least one cell is in the unidirectional FIFO buffer. Parry teaches a FIFO that uses “empty” and “full” flags (abstract; column 2, lines 59-68). A “full” flag is used when it is not the case that space is available for at least one more cell in the unidirectional

buffer, and an “empty” flag is used when it is not the case that there is at least one cell in the unidirectional buffer. It would have been obvious to one of ordinary skill in the art to modify the invention of Takamichi et al. so that it uses “empty” and “full” flags, as in Parry, because such an arrangement prevents unsuccessful read and write operations.

With regard to claims 27, 29, and 30, the limitations that the write clock operates at about 50 megahertz, or that the read clock operates at about 21 or 42 megahertz are obvious design choices. The choice of operating frequency depends in part on the frequencies the devices used by the system can handle.

With regard to claim 31, Takamichi et al. fails to teach that the contents of the buffers can be modified. Parry teaches a data switching system and method for which data may be selectively modified in the buffers (“memory devices”; column 3, lines 1-23). Parry teaches that modification of the buffer contents is particularly useful for ATM to take advantage of any CRC code present in the cell (column 2, lines 40-46). It would have been obvious to one of ordinary skill in the art to modify the invention of Takamichi et al. so that the contents of the buffers can be modified, as in Parry, because such an arrangement would provide an efficient strategy for error detection and/or correction.

With regard to claim 32, it would have been obvious to one of ordinary skill in the art that the inclusion of two switches is a design choice; switches of different kinds can be interconnected as needed.

9. Claims 4-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi et al. and Parry as applied to claim 1 above, and further in view of Kou et al. Claim 49 is rejected

under 35 U.S.C. 103(a) as being unpatentable over Takamichi et al. and Parry as applied to claim 42 above, and further in view of Kou et al. Both Takamichi et al. and Parry teach that their inventions are useful for ATM networks. In particular, Takamichi et al. teaches that the output of the first FIFO buffer (buffer 65 in Fig. 6) goes to an ATM switch (3 in Fig. 1) (column 6, lines 28-32) and the input of the second buffer (buffer 61 in Fig. 6) comes from the same ATM switch. Neither Takamichi et al. nor Parry teach that their inventions could be interfaced with ATM, frame relay, voice, data, T1, E1, T3, E3, OC3, and OC12, or that their inventions could be interfaced with sources of varying bandwidths. Kou et al. teaches an ATM switching system, in which the switch implements an output-buffer type cell-based switching architecture that supports interfaces to ATM OC3/DS3/DS1, SMDS DS3/DS1, and Frame Relay DS1 (see e.g., the abstract and the discussion of Figure 1). In section 7, Kou et al. points out that the ATM backbone will migrate to OC12. An ATM switch can therefore serve as an interface between ATM and frame relay, voice, or data, as well as sources of varying bandwidths such as the bandwidths that are characteristic of T1, E1, T3, E3, OC3, and OC12. It would have been obvious to one of ordinary skill in the art that the inventions of Takamichi et al. and Parry could have been modified so that either the buffers transfer cells between the above listed interfaces; or the buffers transfer cells to and from switches that are connected to one of the above listed interfaces; or the buffers transfer cells to and from switches that can be designed to route cells to an OC12 trunk line; or the buffers transfer cells to and from service modules (which can themselves comprise interfaces) which use T1, E1, T3, E3, OC3, or OC12. It would further have been obvious to one of ordinary skill in the art that using such interfaces is advantageous because it allows the invention to offer more service types to more customers.

Art Unit: 2662

10. Claims 19 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi et al. and Parry as applied to claims 1 and 42, respectively, and further in view of Morgan. Both Takamichi et al. and Parry fail to teach a diagnostic interface that supports a non-destructive read from the bidirectional FIFO unit while at least one cell is being written to and read from the bidirectional FIFO unit. Morgan teaches a circuit that enables the output buffer when data contained in the output buffer is valid. The fact that this circuit, which is a diagnostic interface, performs a nondestructive read on the data is inherent to the invention because the memory device disclosed in Morgan transmits data only after it has been read and found to be valid. It would have been obvious to one of ordinary skill in the art to modify the inventions of Takamichi et al. and Parry so that they employ a diagnostic interface that supports a nondestructive read of the bidirectional buffer because such an arrangement helps to ensure that only valid data will be transmitted.

11. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi et al. and Parry as applied to claim 1, and further in view of Morgan. Neither Takamichi et al. nor Parry discloses an apparatus in which a cell bus controller is coupled to a service module, a master bidirectional FIFO buffer is contained within the cell bus controller, a slave bidirectional FIFO buffer is contained within the service module, and the cell bus controller is connected to a switch. Morgan teaches a system that drives stored data onto a bidirectional bus, where the system comprises a cell bus controller (“initiating means”); a service module (“output means”), which is connected to the cell bus controller; and a master memory device (“memory”) coupled

Art Unit: 2662

to the cell bus controller (claim 1). It would have been obvious to one of ordinary skill in the art that the apparatus disclosed in Morgan could be easily modified so that the master memory device is contained within the cell bus controller because the master memory device in Morgan is coupled to the cell bus controller. The fact that a slave memory device is contained within the service module is inherent to the invention of Morgan because the service module ("output means") is capable of temporarily storing data (claim 1, column 13, lines 56-60). It would have been obvious to one of ordinary skill in the art to modify the inventions disclosed in Takamichi et al. and Parry so that a cell bus controller is coupled to a service module, a master bidirectional FIFO buffer is contained within the cell bus controller, a slave bidirectional FIFO buffer is contained within the service module, and the cell bus controller is connected to a switch, consistent with the invention disclosed in Morgan, because, as taught by Morgan, such an arrangement allows data to be output only when it is valid (abstract).

12. Claims 20, 21, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi et al. and Parry as applied to claims 1 and 42 above, and further in view of Christidou et al. Neither Takamichi et al. nor Parry discloses a bidirectional buffer for which each unidirectional buffer can send cells to the other unidirectional buffer for diagnostic purposes. Christidou et al. teaches a bidirectional queue in which the first unidirectional buffer sends a packet to the second unidirectional buffer with probability p_1 , and the second unidirectional buffer sends a packet to the first unidirectional buffer with probability p_2 . It would have been obvious to one of ordinary skill in the art that modifying the invention of Takamichi et al. or Parry so that the unidirectional buffers route cells to each other with nonzero probabilities, as in

Christidou et al., and so that these probabilities can be set to 0 or 1 as desired would allow diagnostics to be performed on the switch platform; for example, if the delay of cells that traverse the first unidirectional buffer tends to be large, cells currently present in the first unidirectional buffer can be temporarily routed to the second unidirectional buffer in an attempt to find the source of the problem.

13. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi et al. and Parry as applied to claim 22 above, and further in view of Caldara et al. Neither Takamichi et al. nor Parry discloses an invention in which a master bidirectional buffer is inhibited from reading to a slave bidirectional buffer based on feedback from the slave bidirectional buffer. Caldara et al. teaches an invention in which when slave buffers ("output buffers") become filled to a predetermined threshold level a feedback message is provided to the master buffers ("input buffers") to stop the reading ("transmission") of cells from the master buffers to the slave buffers (abstract; column 1, lines 38-50). It would have been obvious to one of ordinary skill in the art to modify the inventions disclosed by Takamichi et al. and Parry by including this feedback because such feedback allows for effective flow control.

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The inventions disclosed in the patents by Denzel et al., Chow et al., Mawhinney, Wills, and Chen, and the articles by Pretty et al., Taylor, and Hunt are pertinent to the claimed invention, but are not relied upon in this action.

Conclusion

15. Any inquiry concerning his communication or earlier communications from the examiner should be directed to Joseph Logsdon whose telephone number is (703) 305-2419. The examiner can normally be reached on Monday through Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached on (703) 305-4744.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

16. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 308-6743

For informal or draft communications, please label "PROPOSED" or "DRAFT".

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Joe Logsdon

Patent Examiner

August 4, 2000



HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2700